Cascaded H-Bridge Low Capacitance Static Compensator with Modular Switched Capacitors

***Abstract*—In this paper, the effect of large double frequency capacitor voltage ripple (CVR) on harmonic performance, efficiency and capacitor lifetime in the cascaded H-bridge low capacitance StatCom (LC-StatCom) is analytically determined. With insight provided by the analysis, an LC-StatCom with modular switched capacitors is proposed that provides a degree of freedom to control the CVR magnitude. The premise of operation is to keep redundant capacitor modules in standby mode when operating with lower currents. In addition, it is shown that by distributing losses between additional dc-side switches and the main H-bridge switches, the proposed concept provides opportunities for choosing an optimal hybrid combination of semiconductor technologies. The proposed concept is evaluated using a simulated 8.5 MVA StatCom and feasibility of the proposed system is confirmed by experiments on a seven-level 0.8 kVA single-phase LC-StatCom prototype.**

***Index Terms*—Cascaded H-bridge, modular switched capacitor, reactive power compensation, StatCom.**

I. Introduction

THE low capacitance StatCom (LC-StatCom), as the name suggests, utilizes relatively low dc-link capacitance, which leads to operation with large capacitor voltage ripple (CVR) [1]–[11]. Phase alignment between the grid voltage and CVR is the key feature utilized in the LC-StatCom concept. By utilizing such phase alignment, LC-StatCom can operate with constant peak capacitor voltage independent of the ripple magnitude [1]. However, this favorable phase alignment only exists in the capacitive operation mode. Hence, LC-StatCom's operation capability in the inductive mode is limited [1]. Nevertheless, symmetrical inductive and capacitive operating capability is achievable by adding an extra thyristor bypassed inductor in series with the filtering inductor [3].

In the capacitive mode, large CVR in the LC-StatCom plays an important role in reducing voltage stress on both capacitors and semiconductors. Large CVR also helps to reduce switching losses due to the reduced average dc-link switching voltage [11]. Furthermore, the CVR has a positive effect on power quality due to improved quality of the synthesized ac-side voltage waveform [9]. Therefore, operation with large CVR in the capacitive mode is favorable. In a conventional LC-StatCom, the controller has no ability to modify the CVR magnitude as it is dictated by the grid's reactive power demand. In practice, LC-StatCom may rarely be required to deliver its rated reactive power continuously. Consequently, LC-StatCom is often forced to operate with sub-optimal CVR magnitude.

The first significant contribution of this paper is analytically determining the effect on harmonic performance, efficiency and capacitor lifetime from CVR. With insight provided by the analysis, a modular switched capacitor (MSC) concept is proposed to add load adaptation functionality to the LC-StatCom. MSCs add an additional degree of freedom to modify the second order CVR magnitude. The controller is able to change the capacitance according to the reactive power demand and maximize the CVR without interrupting the reactive power supplied to the grid. In addition, conduction and switching losses in the main H-bridge semiconductor devices reduce, which helps to mitigate the increase in conduction and switching losses incurred from the additional dc-side switches, as will be shown in this paper. The idea of using only *one* switched capacitor (SC) per sub-module, to reduce semiconductor losses, was proposed in [12], [13] for the modular multilevel converter in high voltage dc application. In this paper, that deals with the LC-StatCom system, the main function of *multiple* switched capacitors per sub-module is to modularize the dc-link capacitance and thereby operate with large CVR at light loading conditions, which will be shown to have capacitor lifetime and harmonic performance benefits.

The organization of this paper is as follows: Section II reviews the cascaded H-bridge (CHB) LC-StatCom concept, Section III analyzes the CVR effect and analytically quantifies its benefits, Section IV introduces the proposed MSC concept, Section V provides simulation results, Section VI provides experimental demonstration, and finally Section VII summarizes the conclusions of this paper.

II. Cascaded H-Bridge LC-StatCom

From the topology point of view, a CHB LC-StatCom does not differ from a conventional CHB StatCom. However, a conventional CHB StatCom uses large capacitors to lower the magnitude of second order CVR, so that the ripple's effect can be ignored (using the average capacitor voltage value) in the analysis and operation of the StatCom [14]–[19].

Fig. 1 shows the main operation principle of an LC-StatCom compared to a conventional StatCom in the capacitive mode. This figure illustrates how the LC-StatCom uses phase alignment between the dc-side voltage ripple and ac-side voltage reference to operate with large CVR without increasing the instantaneous peak capacitor voltage.

Assuming a sinusoidal grid current ($i_g = I\sin\omega t$) and a sinusoidal ac-side voltage ($v = V\cos\omega t$), the capacitor voltage of an H-bridge, v_C, is expressed as follows [1]:

$$v_C = \sqrt{V_{C-max}^2 - \frac{VI}{2\omega C}\left(1-\cos 2\omega t\right)}, \qquad (1)$$

where ω is the angular frequency of the grid voltage, C is the capacitance, and V_{C-max} represents the peak capacitor voltage.

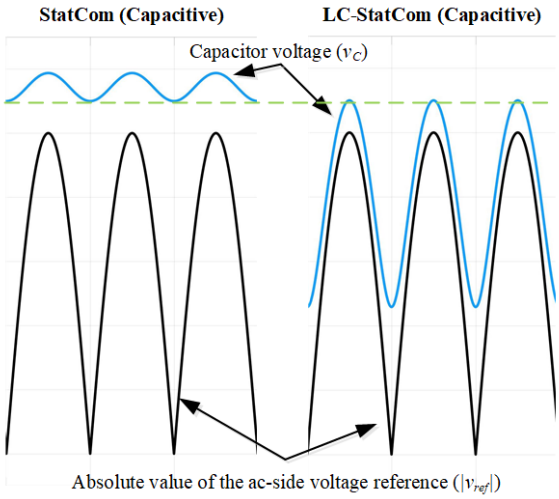


Fig. 1. Conventional StatCom and LC-StatCom operation principles.

In this study, the CVR, r, is defined as

$$r = 1 - \frac{v_{C-min}}{V_{C-max}}, \tag{2}$$

where v_{C-min} represents the minimum instantaneous capacitor voltage. Replacing for v_{C-min} from (1) in (2) yields

$$r = 1 - \frac{\sqrt{V_{C-max}^2 - VI/(\omega C)}}{V_{C-max}}. \tag{3}$$

Rewriting (1) as a function of r by using (3) yields

$$v_{C-p.u} = \sqrt{1 - \frac{r\,(2-r)}{2}\,(1 - \cos 2\omega t)}. \tag{4}$$

$v_{C-p.u}$ in (4) is the normalized value of v_C (using V_{C-max} as the base voltage for normalization).

III. Capacitor Voltage Ripple Benefits

In this section the effect of CVR on power quality, switching and conduction losses, and capacitor voltage lifetime of an H-bridge cell in a StatCom application is analysed.

A. Synthesized Voltage Quality

Quality of the synthesized pulse-width modulated (PWM) voltage, v_{pwm}, is assessed by using total harmonic distortion (THD) as an indicator. The THD of the PWM voltage, THD_v, is defined as follows

$$THD_v = \frac{\sqrt{2V_{pwm-rms}^2 - V^2}}{V}, \tag{5}$$

where $V_{pwm-rms}$ is the rms value and V is the fundamental harmonic component magnitude (peak value) of the PWM voltage waveform. $V_{pwm-rms}$ is given by:

$$V_{pwm-rms} = \sqrt{f_g \int_0^{1/f_g} |v_{pwm}|^2 dt}, \tag{6}$$

where f_g is the grid voltage frequency.

The synthesized PWM voltage of an H-bridge can be either a two-level (bipolar modulation) or a three-level (unipolar modulation) waveform. In the following, the effect of CVR on THD_v for both PWM waveform types is analysed.

Two-level PWM waveform: In a two-level PWM waveform, the PWM voltage is generated by using two voltage levels i.e. $\pm v_C$, as a result $|v_{pwm}| = |v_C|$. Therefore, from (6), $V_{pwm-rms} = V_{C-rms}$ irrespective of the switching frequency or modulation index (V_{C-rms} is the rms value of v_C). From (4),

$$V_{C-rms-p.u}^2 = 1 - \frac{r\,(2-r)}{2}. \tag{7}$$

Therefore, THD_v as a function of r is

$$THD_v = \frac{\sqrt{(r-1)^2 + 1 - V_{p.u}^2}}{V_{p.u}} \tag{8}$$

As it can be seen from (8) by increasing r ($0 < r < 1$), THD_v decreases.

Three-level PWM waveform: In a three-level PWM waveform, the PWM voltage is generated by three voltage levels i.e. $\pm v_C$ and 0. In this case, the presence of the zero voltage state makes the calculation of $V_{pwm-rms}$ more complex. $|v_{pwm}|$ is a peicewise function that oscillates between zero and v_C in such a way that at any switching cycle its average value is equal to $|v_{ref}|$, where v_{ref} is the desired ac-side voltage reference. Therefore,

$$V_{pwm-rms} = \sqrt{f_g \sum_{n=1}^{f_s/f_g} \int_{(n-1)/f_s}^{(n-1+d(n))/f_s} v_C^2 dt}. \tag{9}$$

In (9), f_s is the switching frequency and the duty cycle, d, is

$$d(n) = \frac{|v_{ref}(n)|}{v_C(n)}. \tag{10}$$

Assuming v_{ref} and v_C remain constant during a switching period, (9) can be rewritten as:

$$V_{pwm-rms} = \sqrt{\frac{f_g}{f_s} \sum_{n=1}^{f_s/f_g} v_C(n)|v_{ref}(n)|}. \tag{11}$$

From (11), it can be seen that $V_{pwm-rms}$ is equal to the square root of the average of $v_C|v_{ref}|$. Therefore,

$$THD_v = \frac{\sqrt{2\overline{v_{C-p.u}|v_{ref-p.u}|} - V_{p.u}^2}}{V_{p.u}}, \tag{12}$$

where the overline notation shows the average (over a fundamental period) value of a quantity. As it can be seen from (4), by increasing r, the average capacitor voltage decreases. Hence, by increasing r, THD_v in (12) decreases.

As an example, Fig. 2 shows the variation of THD_v for $v_{ref-p.u} = 0.9\cos\omega t$.

B. Switching Loss

The instantaneous switching loss, e_s, is assumed to be proportional to both the magnitude of capacitor voltage and the grid current at the switching instant [20]. Hence, increasing the CVR will directly affect the switching loss as follows:

$$e_s = e_{s-n} v_{C-p.u} |i_{g-p.u}|, \tag{13}$$

where e_{s-n} represents the switching loss at $v_{C-p.u} = 1$ and $i_{g-p.u} = 1$.

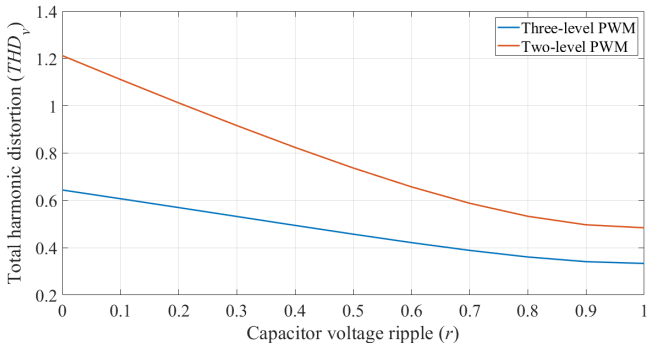


Fig. 2. THD in two- and three-level PWM voltage waveforms.

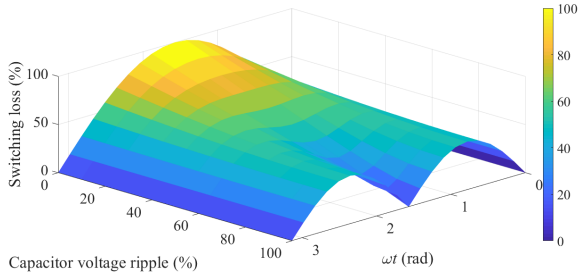


Fig. 3. Switching loss in the capacitive operating mode as a function of the maximum CVR at rated current.

As an example, in Fig. 3 the switching losses are shown as a percentage point of e_{s-n} for $I_{p.u} = 1$ ($i_{g-p.u} = \sin\omega t$). As it can be seen, the losses reduce significantly by increasing r especially when the instantaneous current is high (because in capacitive mode, when the grid current is at its peak, the capacitor voltage is at its minimum).

It is worth noting that the conduction losses remain unaffected by the CVR. CVR changes the duty-cycle and affects the duration of bypass mode (zero PWM voltage state, where a diode and a controllable switch conduct and, as a result, conduction time is evenly distributed between the diodes and controllable switches). However, considering symmetry between the rectifying half-cycle (two diodes conduct) and inverting half-cycle (two controllable switches conduct), the conduction time during active mode ($\pm v_C$ PWM voltage state) over a cycle is still evenly distributed between the controllable switches and diodes. Therefore, the two active and bypass operating modes from conduction losses perspective over a full cycle are identical and as a result the conduction losses remains unaffected by the CVR.

Remark: In this analysis, the change in CVR is due to the capacitance change (i_g is assumed to remain unchanged).

C. Capacitor Lifetime

Operating with lower average capacitor voltage (higher r) is beneficial to improve semiconductor reliability as it will reduce cosmic failure rate of power semiconductors [21]. At the same time, as demonstrated in this section, a larger CVR is expected to increase the capacitor lifetime. This study assumes utilization of film capacitor technology in the dc-link, as electrolytic capacitors are not needed in the LC-StatCom due to the low capacitances values required to produce large voltage ripples.

The life expectancy for film capacitors is approximated by the following equation [22]:

$$H = H_0 \frac{V_0^7}{\overline{v_C^7}} \times 2^{(T_m - T_a - \Delta T)/10}. \tag{14}$$

In (14), H represents the expected lifetime, which is dependent on the operating and environmental conditions (humidity dependency is neglected). It is noted that H is dependent on v_C^7, which in the LC-StatCom is a time-varying quantity. Therefore, to evaluate the expected lifetime, the average of the term v_C^7 must be determined, which is defined as $\overline{v_C^7}$. T_m and T_a are the maximum temperature rating of the capacitor and the ambient temperature, respectively. ΔT represents the temperature increase due to power losses on the equivalent series resistance (ESR), V_0 is the maximum continuous voltage rating, and H_0 is the reference lifetime of the capacitor (measured at $v_C = V_0$ and $\Delta T = 0$). ΔT is a function of the rms capacitor current, I_{C-rms}, as follows,

$$\Delta T = \frac{I_{C-rms}^2 R_C}{A\beta}, \tag{15}$$

where, A is the surface area of the capacitor, R_C is the capacitor ESR, and β is the thermal constant.

In this section, the effect of r on H is studied based on a reference value, H_n, which is defined as the lifetime of a capacitor in an LC-StatCom H-bridge that produces 100% CVR ($r = 1$) at the reference operating point i.e. $v_{ref-p.u} = \cos\omega t$ and $i_{g-p.u} = \sin\omega t$. At this operating condition, the capacitor is always conducting ($d = 1$ from (10)) and as a result the rms capacitor current is equal to the rms grid current ($I_{C-rms} = I_n/\sqrt{2}$, where I_n is the peak value of nominal grid current). Therefore,

$$H_n = 3.435K2^D, \tag{16}$$

where

$$K = H_0 \frac{V_0^7}{V_{C-max}^7} \times 2^{(T_m - T_a)/10}, \tag{17}$$

and

$$D = \frac{-I_n^2 R_{Cn}}{20A\beta}. \tag{18}$$

In (17) V_{C-max} appears due to utilization of normalized capacitor voltage (from (16), for $r = 1$, $1/\overline{v_{C-p.u}^7} = 3.435$).

In (18), the ESR of the reference capacitor is represented as R_{Cn}. At a given operating condition, r is dependent on C as seen in (3) ($C^{-1} \propto r(2-r)$). Also as $R_C \propto C^{-1}$, then $R_C \propto r(2-r)$. Therefore, $R_C = R_{Cn} r(2-r)$.

The choice of switching scheme also affects the capacitor aging through I_{C-rms}. In the following, both two-level and three-level PWM schemes are considered.

Two-level PWM scheme: In a two-level PWM scheme, the capacitor is never bypassed and the instantaneous capacitor current magnitude is equal to the instantaneous grid current magnitude ($|i_C| = |i_g|$). In this case, I_{C-rms} is independent of the CVR (assuming a sinusoidal grid current, $I_{C-rms} =$

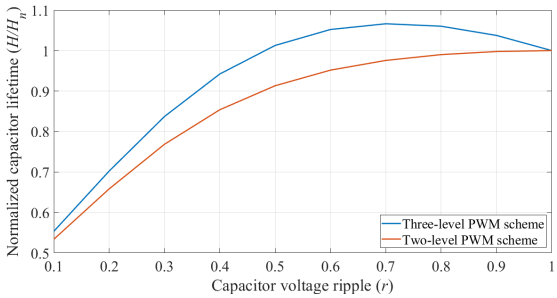


Fig. 4. Effect of the CVR on capacitor lifetime at rated operating condition and assumption of maximum 10°C temperature increase.

$I_n/\sqrt{2}I_{p.u}$). Therefore, the effect of r on the capacitor lifetime at rated current ($I_{p.u} = 1$) is as follows

$$\frac{H}{H_n} = \frac{2^{D(r(2-r)-1)}}{3.435 \times \overline{v_{C-p.u}^7}}, \tag{19}$$

where, $v_{C-p.u}$ is given in (4).

Three-level PWM scheme: In the three-level PWM scheme, the capacitor current, i_C, at zero voltage state is zero (otherwise $|i_C| = |i_g|$). Therefore, for a three-level modulation scheme, I_{Crms} can be derived in a similar way to $V_{pwm-rms}$ (as in 9) as follows:

$$I_{C-rms} = \sqrt{f_g \sum_{n=1}^{f_s/f_g} \int_{(n-1)/f_s}^{(n-1+d(n))/f_s} i_g^2 dt}. \tag{20}$$

Replacing (10) in (20) and assuming a constant d and i_g within a switching period yields

$$I_{C-rms} = \sqrt{\frac{f_g}{f_s} \sum_{n=1}^{f_s/f_g} \frac{|v_{ref}(n)|}{v_C(n)} i_g(n)^2}. \tag{21}$$

Hence,

$$I_{C-rms} = \sqrt{\overline{\frac{|v_{ref}|}{v_C}}\, i_g^2}. \tag{22}$$

Therefore, at the reference condition ($v_{ref-p.u} = \cos\omega t$, $i_{g-p.u} = \sin\omega t$), the effect of r on the capacitor lifetime is

$$\frac{H}{H_n} = \frac{2^{D(2r(2-r)\overline{\sin^2\omega t|\cos\omega t|/v_{C-p.u}}-1)}}{3.435 \times \overline{v_{C-p.u}^7}}, \tag{23}$$

where, $v_{C-p.u}$ is given in (4).

In Fig. 4 as an example, H/H_n using (19) and (23) is shown. In this example $D = -0.5$, which corresponds to the maximum temperature increase of 10°C, is used. Therefore, by operating with a larger CVR not only the required capacitor is smaller, its lifetime is expected to be longer as well.

IV. Modular Switched Capacitor

A. Circuit Topology

Given the importance of the CVR on the LC-StatCom performance, the system would benefit if it had a degree of freedom to maximise the capacitor voltage ripple magnitude (r). However, in the conventional LC-StatCom hardware structure there is no mechanism to do so. Hence, as the power decreases, r decreases as well, which means the LC-StatCom will be forced to operate with a small CVR when delivering powers less than the nominal power. In order to overcome this drawback, in this section, MSC is introduced to add a degree of freedom to control r. The MSC concept has been extended from the SC concept proposed in [12], [13]. In Figs. 5(a) and (b), the SC solution and the proposed MSC are shown, respectively.

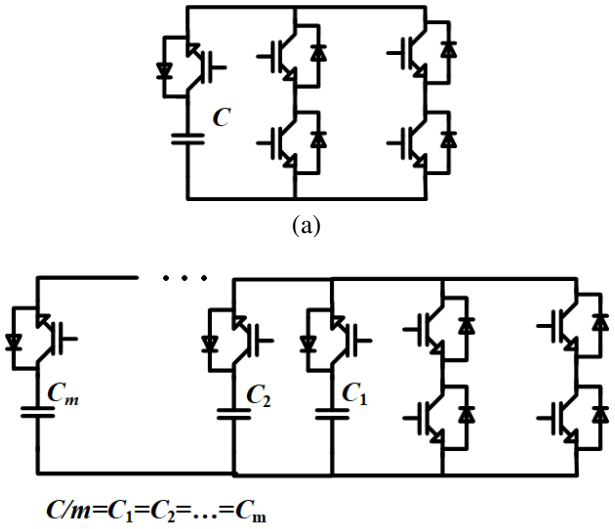


Fig. 5. (a) H-bridge cell with SC, and (b) with the proposed MSC.

The equivalent dc-link capacitance in MSC, C', is controlled as a function of the rms current as given in (24), where m represents the number of parallel connected capacitor branches, as shown in Fig. 5(b).

$$C' = \begin{cases} \lfloor mI_{p.u} + 1 \rfloor C/m & , \quad 0 \le I_{p.u} < 1 \\ C & , \quad I_{p.u} = 1 \end{cases}. \tag{24}$$

In this equation, $f(x) = \lfloor x \rfloor$ is the floor function (f is the largest integer less than or equal to x). C' in (24) is reduced as the rms capacitive current decreases. As an example, when $0 \le I_{p.u} < (1/m)$, then $1 \le mI_{p.u} + 1 < 2$, which leads to $C^{'} = C/m$ and similarly $C^{'} = 2C/m$ for $(1/m) \le I_{p.u} < (2/m)$ and so on. Consequently, r remains close to its maximum value throughout the capacitive operating region of the LC-StatCom.

In this scheme, when a dc-side switch is off, its corresponding capacitor will eventually charge up to V_{C-max} through the anti-parallel diode and remains in standby mode. The voltage of the online capacitors on the other hand, will continue to oscillate. When the rms grid current increases, additional capacitors will switch on at the next peak capacitor voltage crossing to cope with a larger reactive power demand. Conversely, if the rms grid current reduces, the redundant capacitors will enter standby mode so that the remaining online capacitors can operate with a larger ripple.

The process of activating and deactivating the kth capacitor module, is illustrated in Fig. 6. In this figure, the highlighted

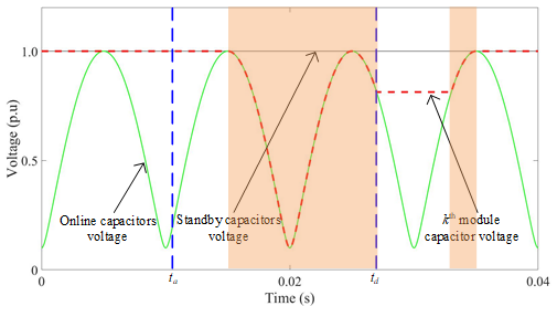


Fig. 6. Activation and deactivation process of kth capacitor module (highlighted regions show where the capacitor module is active and t_a and t_d are the desired activation and deactivation times, respectively).

areas indicate the kth capacitor module is online. As it can be seen, a capacitor can be activated safely (without any inrush currents) at the peak voltage crossing where all the capacitors have the same voltage, i.e V_{C-max}. Therefore, after receiving the activation command at t_a the capacitor waits until the next peak voltage crossing before coming online. On the other hand, deactivation can happen at any time, e.g. at t_d, and the deactivated capacitor voltage is charged back to V_{C-max}.

B. Loss Analysis

It was shown in [12], [13] that a benefit of the SC concept is the ability to reduce conduction losses in the H-bridge. This is possible because when the zero-voltage state is applied in the H-bridge (bypass mode), the dc-side switch is turned off to disconnect the capacitor, which allows all four H-bridge switches (or their anti-parallel diodes depending on the current direction) to conduct simultaneously and therefore, the current splits between the upper and lower conduction paths in each switching leg resulting in reduction in equivalent resistance by 50%. This concept is demonstrated in Fig. 7. This current splitting is retained in the MSC concept, and the resulting decrease in conduction loss helps to mitigate increases in semiconductor losses incurred by addition of the dc-side switches.

Effectiveness of current splitting during bypass mode to reduce H-bridge conduction losses can be evaluated analytically. In a conventional H-bridge cell during bypass mode the current flows through a diode and a controllable switch. Therefore, at the n^{th} switching period, ε_0, which represents the dissipated energy in H-bridge semiconductors during the bypass mode is:

$$\varepsilon_0(n) = \frac{1-d(n)}{f_s}|i_g(n)|[v_S(|i_g(n)|) + v_D(|i_g(n)|)]. \quad (25)$$

In (25), v_S and v_D depend on the current magnitude and represent the voltage drop across the switch and the diode, respectively. With current splitting, the conduction losses (during bypass mode) on the H-bridge is

$$\varepsilon_0'(n) = \frac{1-d(n)}{f_s}|i_g(n)|[v_S(\frac{|i_g(n)|}{2}) + v_D(\frac{|i_g(n)|}{2})]. \quad (26)$$

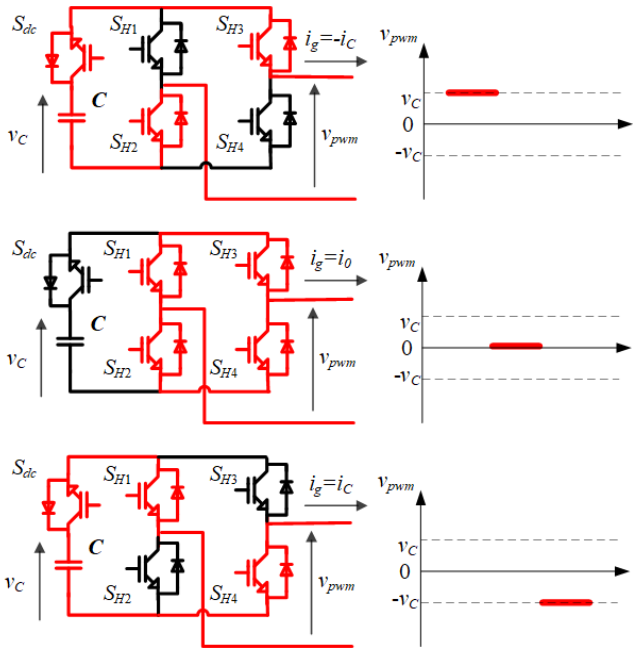


Fig. 7. Conduction paths for each switching state in an H-bridge cell with dc-side switch.

Therefore, the conduction power loss reduction on an H-bridge, Δp_0, as a result of having the dc-side switch is calculated as,

$$\Delta p_0 = f_g \sum_{n=1}^{f_s/f_g} (\varepsilon_0(n) - \varepsilon_0'(n)). \quad (27)$$

Due to the nonlinear nature of $v_S(i_g)$ and $v_D(i_g)$, (27) needs to be solved numerically. However, a closed form solution for (27) can be found by approximating $v_S(i_g)$ and $v_D(i_g)$ with linear functions such as,

$$v_{S/D} = V_{S/D} + R_{S/D}|i_g|, \quad (28)$$

where $V_{S/D}$ and $R_{S/D}$ represent constant threshold voltage drop and conducting resistance of the switch/diode, respectively. The conduction loss using this simplified model has two components, one due to the constant threshold voltage proportional to the dc component of the rectified current, and the other due to the resistance that is proportional to the square rms current.

In three-level PWM, as shown in Fig. 7, i_g will either flow through the capacitor or return through the bypass route. This bypassed portion of the current is denoted as i_0.

$$i_0 = \begin{cases} 0 & , \quad v_{pwm} = \pm v_C \\ i_g & , \quad v_{pwm} = 0 \end{cases}. \quad (29)$$

Current magnitude in the bypass mode, $|i_0|$, is easily calculated by subtracting the capacitor current magnitude, from the grid current magnitude ($|i_0| = |i_g| - |i_C|$). Therefore,

$$I_{0-rms}^2 = I_{g-rms}^2 - I_{C-rms}^2, \quad (30)$$

and

$$\overline{|i_0|} = \overline{|i_g|} - \overline{|i_C|}. \quad (31)$$

In (30), I_{g-rms} is the grid current rms value, I_{0-rms} represents the rms value of i_0, and I_{C-rms} is given in (22). Therefore, assuming a sinusoidal grid current (30) can be rewritten as a function of r as follows,

$$I_{0-rms}^2 = \frac{I^2}{2} - \overline{\frac{I^2 V_{p.u} \cos\omega t \sin^2 \omega t}{\sqrt{1-r(2-r)(1-\cos 2\omega t)/2}}}. \quad (32)$$

The average rectified sinusoidal grid current is I/π, and the average rectified capacitor current is

$$\overline{|i_C|} = |4 f_g C \int_0^{1/(4f_g)} \frac{dv_C}{dt} dt|. \quad (33)$$

From (4) and (33),

$$\overline{|i_C|} = 4 f_g C r V_{C-max}. \quad (34)$$

Therefore, (31) can be rewritten as a function of r as follows,

$$\overline{|i_0|} = \frac{I}{\pi} - 4 f_g C r V_{C-max}. \quad (35)$$

The saving in H-bridge conduction losses due to current splitting can now be expressed in the following closed form:

$$\Delta p_0 = \frac{R_S + R_D}{2} I_{0-rms}^2, \quad (36)$$

where, I_{0-rms} is given in (32). The additional conduction losses on the dc-side semiconductor, p_{dc}, is as follows:

$$p_{dc} = \frac{R_{S-dc} + R_{D-dc}}{2} I_{C-rms}^2 + \frac{V_{S-dc} + V_{D-dc}}{2} \overline{|i_C|}, \quad (37)$$

in which, $\overline{|i_C|}$ is given in (34) and the subscript dc refers to parameters of the dc-side controllable switch and diode.

Distribution of the switching losses is an additional feature of the MSC circuit. At any switching instant, the current commutates from the dc-side switches to the H-bridge switches and vice versa, which allows for even distribution of switching losses between the dc-side and H-bridge switches. For instance, in Fig. 7, when the PWM output voltage changes from $+v_C$ to 0, the current commutates from the dc-side switch to two ac side switches (S_{H1} and S_{H4}). Conversely, when the PWM voltage returns from 0 to $+v_C$, the current commutates from S_{H1} and S_{H4} to the dc-side switch. Even though at every switching instance two H-bridge switches change status, they do so with half the grid current magnitude, which is somehow equivalent to switching one switch with the full current. Therefore, the switching losses on the main H-bridge semiconductors is 50% lower, compared to a conventional H-bridge without MSC, due to utilization of dc-side switches. This characteristic presents opportunities to reduce the overall switching losses considerably (compared to an H-bridge without dc-side switches) by using faster, lower rms current switches, such as wide-bandgap semiconductors on the dc-side. Furthermore, as the H-bridge switches are required to commutate half of the grid current, their turn off current is 50% lower, which allows for utilization of smaller gate driver circuits for high power switches such as IGCTs and GTOs.

TABLE I
PARAMETERS OF THE SIMULATION SYSTEM

Symbol	Parameter	Value
V_{g-rms}	Grid voltage rms value	6 kV
C	Capacitance (per module)	1.7 mF
L	Filter inductance	1 mH
f_s	Switching frequency (per H-bridge)	500 Hz
V_{C-max}	Peak capacitor voltage	1.9 kV
r_m	Maximum capacitor voltage ripple	75 %
f_g	Grid frequency	50 Hz
S	Nominal power	8.5 MVA
N	Number of H-bridges	5
m	Number of capacitor modules (per H-bridge)	2

V. SIMULATION STUDY

Simulations in this section are designed to evaluate the PWM voltage quality and loss distribution among switches in an LC-StatCom H-bridge module with MSC and confirm validity of the theoretical prediction. An eleven-level single-phase CHB StatCom with parameters given in Table I is simulated in MATLAB/Simulink.

In the following results, a conventional LC-StatCom (no dc-side switches and a constant 3.4 mF capacitance per H-bridge) with 5SNA 2000K451300 IGBT switches (2000 A, 4500 V) is assumed. The proposed MSC concept with two capacitor modules is also simulated, in which two extra 5SNA 1200E330100 IGBT switches (1200 A, 3300 V) are used in the dc-side. In theory, the blocking voltage of the dc-side switches should be equal to the ones in the H-bridge. However, here the aim is to use available switches from the same manufacturer that closely satisfy both current and voltage requirements and, at the same time, are comparable with ratings of SiC hybrid IGBTs used for an alternative design given in the following of this section.

In the simulations, the semiconductors characteristics were accurately modelled based on datasheet I-V curves for $120°$C junction temperature in order to have a realistic assessment of the losses.

Fig. 8 shows improvement in the quality of the generated PWM voltage by Cell 1, as a result of increased CVR. In this simulation three-level phase shifted PWM strategy is utilized. As it can be seen, the simulation THD figures closely match the analytic predictions based on (12).

In Fig. 9, the estimated saving in H-bridge conduction losses using (36) and added dc-side switch conduction losses using (37) are compared to the simulation results. As it can be observed the analytical solutions are able to predict the conduction losses with satisfactory accuracy.

The share of conduction and switching losses on Cell 1 for each of the cases is shown in Fig. 10. As can be seen, by using dc-side switches the conduction losses on the main H-bridge switches reduce, which is the result of having two parallel current paths during bypass mode. This saving on main H-bridge conduction losses helps to mitigate the effect of added conduction losses on the dc-side switches as demonstrated in

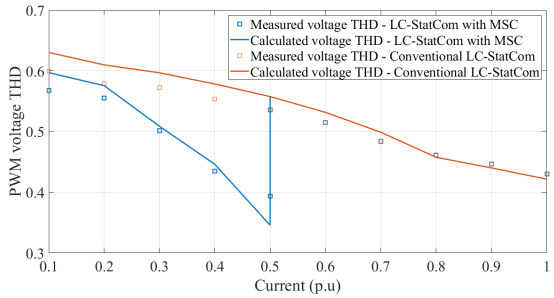


Fig. 8. Cell 1 PWM voltage THD.

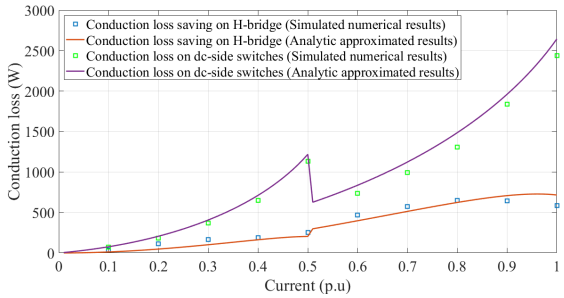


Fig. 9. Predicted and simulated conduction loss saving on H-bridge 1 due to current splitting at bypass mode, and predicted and simulated conduction loss on the dc-side switches.

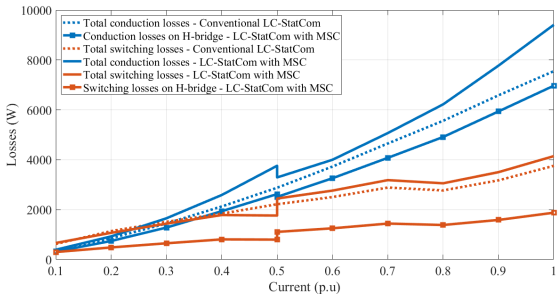


Fig. 10. Distribution of conduction and switching losses on a cell for a conventional LC-StatCom and MSC LC-StatCom.

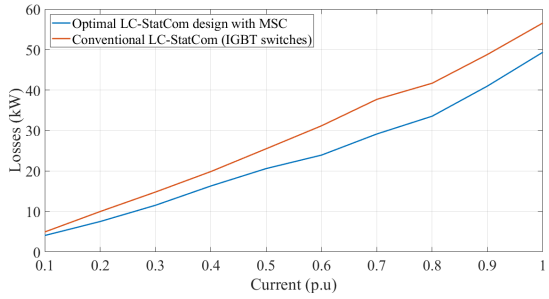


Fig. 11. Total losses for the LC-StatCom with MSC based on IGCT and SiC hybrid IGBT, and a conventional LC-StatCom based on IGBT.

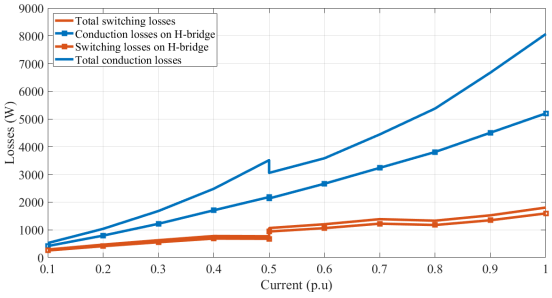


Fig. 12. Distribution of conduction and switching losses on a cell in the optimized design using IGCT and SiC hybrid IGBT.

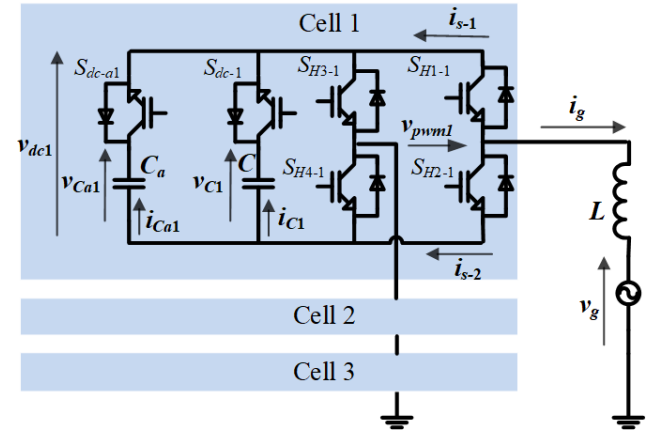
Fig. 9. The switching loss on the main H-bridge is exactly half when dc-side switches are employed. By using the same type of switch on both the dc-side and H-bridges, the overall switching loss does not change considerably for high currents as seen in Fig. 10. At lower currents, the switching loss for MSC equipped LC-StatCom is slightly lower, which is a result of operating with larger CVR.

The results of this simulation highlight opportunities to utilize a hybrid combination of semiconductor devices. As stated above, in the proposed MSC concept, half of the active switching transitions are moved from the H-bridge switches to the dc-side switches. Therefore, it is feasible to utilize H-bridge semiconductors that have been optimized to reduce conduction loss (such as IGCTs). It is also noted that utilizing a modularized structure on the dc-side allows for utilization of devices with lower rms current ratings (as they do not conduct when the H-bridge is bypassed), making it potentially feasible to utilize emerging wide-bandgap devices.

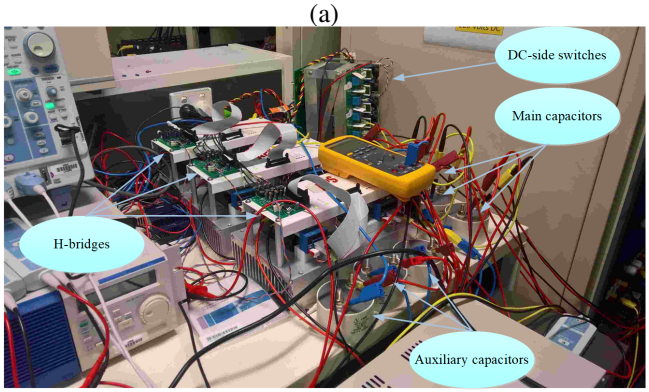
As an example, a design based on 5SHY 35L4522 IGCT switches (4500 V, 2100 A) with 5SDF 20L4520 anti parallel fast recovery diodes (4500 V, 1970 A) for the H-bridge and 5SDF 20L4520 SiC hybrid IGBT switches (1700 V, 1200 A) for the dc side (two switches in series for each capacitor module to meet the voltage blocking requirement) reduces the overall losses compared to the conventional LC-StatCom as shown in Fig. 11. The conduction losses on the H-bridge in this design reduce considerably (approximately 25% at rated power compared to the IGBT based design) due to utilization of IGCT switches optimized for lower conduction losses, as shown in Fig. 12. Additionally, utilization of SiC hybrid IGBT switches on the dc-side reduces the total switching losses significantly (approximately 55% at rated power compared to the IGBT based design). At the same time, having the dc-side switches reduces the required turn off current rating of the IGCT switches by 50%.

VI. Experimental Demonstration

Given that a three-phase CHB StatCom is composed of three individual single-phase CHB converters and that the effect of the MSC on all the phases is identical, in this section, for simplicity, a single-phase CHB StatCom setup is used for demonstration purposes. The circuit diagram and an overview of the experimental system are shown in Fig. 13. The parameters of the experimental system are given in Table II. In this setup, three POWEREX PP75B060 (600 V dc, 75 A rms current rating) H-bridge converters were connected in series to construct a seven-level CHB converter. Compared to the ratings of the experimental setup (given in Table II),



(a)



(b)

Fig. 13. (a) Circuit diagram of the experimental LC-StatCom with MSC, and (b) experimental setup overview.

TABLE II
PARAMETERS OF THE EXPERIMENTAL SYSTEM

Symbol	Parameter	Value
V_{g-rms}	Grid voltage rms value	110 V
C	Capacitance (per module)	0.26 mF
L	Filter inductance	5 mH
f_s	Switching frequency (per H-bridge)	2000 Hz
V_{C-max}	Peak capacitor voltage	75 V
r_m	Maximum capacitor voltage ripple	40 %
f_g	Grid frequency	50 Hz
S	Nominal power	800 VA
N	Number of H-bridges	3
m	Number of capacitor modules (per H-bridge)	2

which was limited by the ratings of the inductor and isolating transformer, the utilized H-bridge converters are significantly overrated. Therefore, in order to achieve the desired CVR, the existing electrolytic dc capacitors in the converters were removed and replaced by smaller modularised switched film capacitors. The control functions were all implemented in a dSPACE system and PWM commands were transferred to the gate drivers by using custom made optical interfaces.

The control system for the proposed LC-StatCom is very similar to the conventional LC-StatCom with fixed capacitors

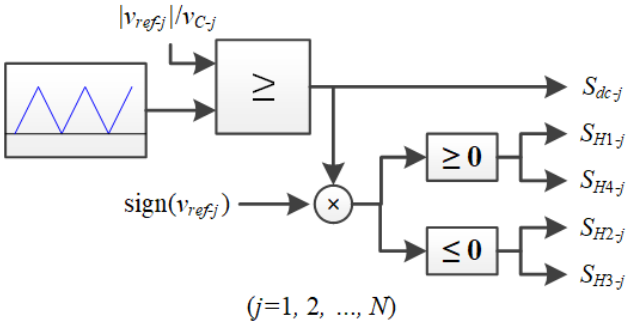


Fig. 14. PWM module for an H-bridge with dc-side switches.

[1]. The control system uses C'/C, as a feedforward signal to compensate for the effect of varying capacitance by scaling the output of the cluster capacitor voltage controller (As $m = 2$, the threshold to activate or deactivate the additional capacitor module is set at $I_{p.u} = 0.5$). Hence, when the capacitance changes, the active component of the grid reference current (output of the cluster voltage controller) changes accordingly due to the added feedforward compensating gain to keep the dynamic of this control loop unchanged.

In this paper, phase shifted triangular carrier PWM method is used to generate the desired ac-side voltage. Fig. 14, shows the logic behind controlling the switches in a cell, e.g. Cell j. As can be seen, the main PWM task is performed by the dc-side switches. All the switches in active capacitor branches will share the same gate control signal, S_{dc}, and those in standby capacitor branches will remain off. When $S_{dc} = 0$, all H-bridge side switches will turn on to create parallel paths for the current to flow. On the other hand, when $S_{dc} = 1$, depending on the sign of v_{ref}, $S_{H1,4}$ or $S_{H2,3}$ will turn on to apply the dc voltage with correct polarity.

In Fig. 15, stable operation of the proposed LC-StatCom system is demonstrated. As can be seen from this figure, changing the capacitor module status from standby to active happens smoothly and does not interrupt operation of the LC-StatCom. Furthermore, by increasing the amount of peak reactive current from 4 A to 9 A, CVR magnitude on the active capacitors remains almost unchanged as desired. When the current is low, the redundant capacitors remain in standby mode at V_{C-max}. Any control action that requires additional capacitors to come online is delayed (maximum half a cycle) until the next capacitor voltage peak crossing. In other words, in Fig. 15, after receiving the reactive power increase command in the highlighted area, the controller waits and only executes the command at t_0 where the needed capacitors can come online safely without undergoing any transient. It is worth noting that this delay time can be easily avoided in a delta-connected three-phase system by injecting some circulating current to circulate excess reactive power among the phases until all capacitors come online. As an example, Appendix A, illustrates how a simple third order harmonic circulating current can help to circulate energy among the phases to achieve this functionality.

The capacitor switching functionality of the proposed LC-

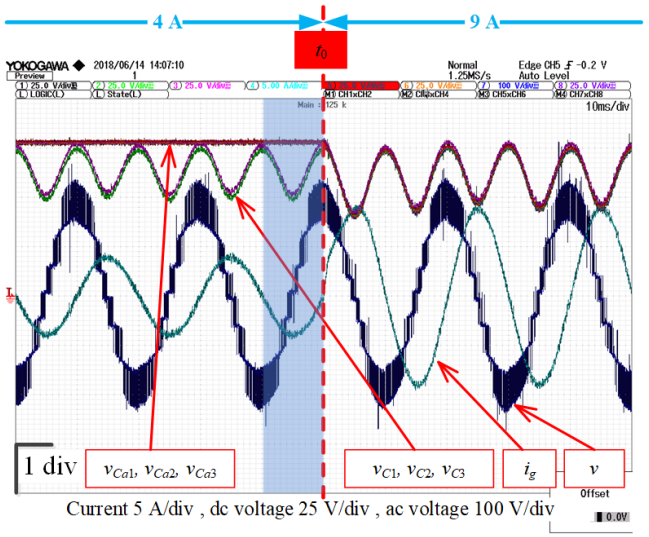


Fig. 15. Transient operation of the proposed LC-StatCom during step reactive current change from 0.4 p.u to 0.9 p.u (control action received in the highlighted area is delayed and executed at t_0).

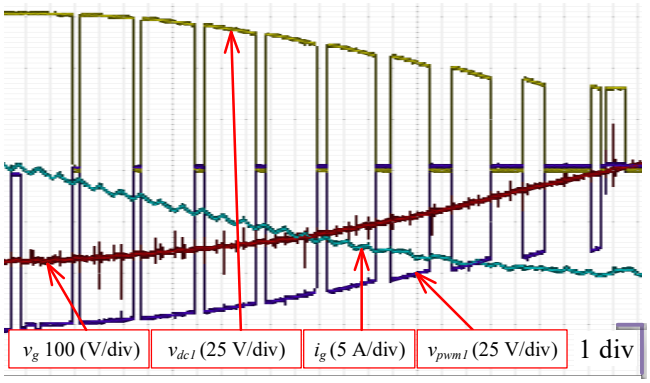


Fig. 16. Demonstration of capacitor switching to generate PWM voltage.

StatCom is shown in Fig. 16 for Cell 1. The LC-StatCom is delivering its rated power. The sensor locations for measuring each quantity in this figure are shown in Fig. 13. As can be seen, the dc-link voltage follows the rectified ac-side voltage waveform because the dc-side switches block the capacitor voltage. Such capacitor switching action does not produce any significant current disturbances on the capacitors as shown in Fig. 17. Furthermore, the result shows even distribution of current between the two capacitor branches. Even distribution of current between the online capacitors ($i_C = Cdv_C/dt$) was expected because both capacitors have the same capacitance and equal voltage. However, small discrepancies at high frequencies might occur due to differences in stray inductances as seen in this Figure. Therefore, in a high power system, it is important to minimize (and equalize) the stray inductances in both parallel paths to avoid issues with overcurrent. During H-bridge bypass mode, the dc-side voltage becomes zero and the ac current splits between the H-bridge's upper and lower switches as shown in Fig. 18.

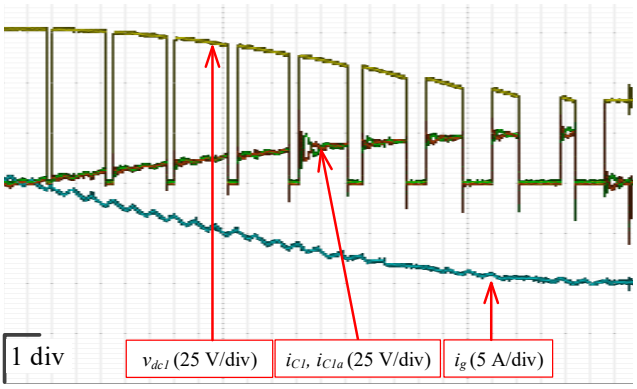


Fig. 17. Capacitors current profile for Cell 1 at rated power.

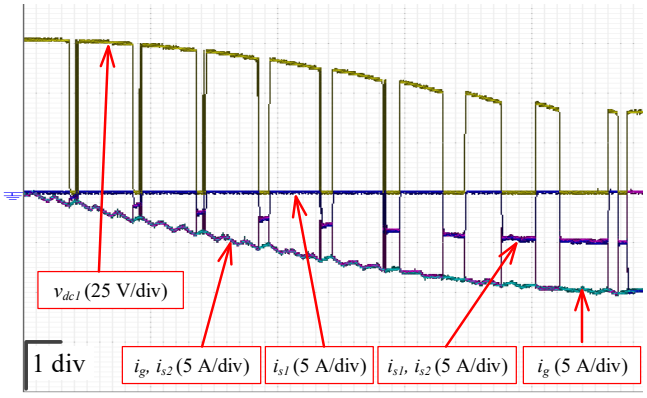


Fig. 18. Demonstration of current split between upper and lower switches of Cell 1 H-Bridge when the capacitor switch disconnects.

VII. Conclusion

This paper analytically derives the effect of CVR on LC-StatCom harmonic performance, switching loss, and capacitor lifetime. It is also shown that CVR can be maximised throughout the capacitive region by modularising the capacitors. The effect of using the MSC on switching and conduction loss distribution was analysed and demonstrated via simulation results. The experimental results presented in this paper on a 0.8 kVA single-phase seven-level LC-StatCom prototype confirm feasibility of the proposed MSC concept. Given the additional costs and complexities associated with the additional switches as well as control issues, further studies are needed to complement the findings of this paper and evaluate its practical value.

VIII. Appendix A: Circulating Current Calculation

The aim of injecting a circulating current here is to prevent the excess double frequency oscillating power from going into the capacitors. Assuming the online capacitors can provide maximum I_m reactive power, and the controller is demanding $I = I_m + dI$, the excess double frequency oscillating power needs to circulate among the phases. Assuming the circulating current only contains third order harmonic and neglecting the

voltage drop associated with this circulating component, the instantaneous per-phase power is

$$p = V\cos\omega t((I_m + dI)\sin\omega t + I_{circ}\sin(3\omega t + \phi_{circ})). \tag{38}$$

In (38), I_{circ} and ϕ_{circ} are the magnitude and phase angle of the circulating current, respectively. The double frequency component of p, represented by $p_{2\omega}$ is

$$p_{2\omega} = 0.5V((I_m + dI)\sin 2\omega t + I_{circ}\sin(2\omega t + \phi_{circ})) \tag{39}$$

Therefore, if $\phi_{circ} = 0$ and $I_{circ} = -dI$, all the excessive double line frequency power will circulate among the phases and will not appear on the capacitor voltage.

The capacitor voltage expression in presence of such circulating power is

$$v_C = \sqrt{V_{C-max}^2 - \frac{VI_m}{2\omega C}(1-\cos 2\omega t) + \frac{VdI}{4\omega C}(1-\cos 4\omega t)}. \tag{40}$$

As can be seen, some distortion due to fourth order oscillating power now appears on the capacitor voltage. This distortion has a positive effect on the capacitor voltage and increases the average dc voltage magnitude. For $0.5I_m < dI$, the peak capacitor voltage also increases beyond V_{C-max} given as ΔV_m,

$$\Delta V_m = (\sqrt{V_{C-max}^2 + V\frac{(2dI - I_m)^2}{8\omega C dI}} - V_{C-max})\frac{C}{C_a + C}. \tag{41}$$

In (41), C_a represents the additional capacitance that comes online when v_C reaches V_{C-max}, which helps reducing ΔV_m. This voltage increase enforces a theoretical upper limit on the magnitude of circulating current (other than the limits imposed by the semiconductors current rating).

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